REMARKS

In response to the Office Action dated 1 April 2003, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 1-41 and 43-45 are pending in the application, and are rejected. None of the claims has been amended.

Rejection of Claims Under §103

Claims 1-2, 4-6, 8-10, 12-28, 30-41, and 43-45 were rejected under 35 USC § 103(a) as being unpatentable over Matsumura et al. (U.S. Patent No. 5,991,232, Matsumura) in view of Manning (U.S. Patent No. 6,032,274). The applicant respectfully traverses.

Matsumura issued on 23 November 1999, which is after the 29 January 1999 filing date of the above-identified application. Manning issued on 29 February 2000, which is after the 29 January 1999 filing date of the above-identified application. The applicant does not admit that either Matsumura or Manning is prior art, and reserves the right to swear behind Matsumura or Manning, or both, at a later date.

The MPEP states the following with regard to rejections under 35 USC § 103:

"To establish a *prima facie* case of obviousness ... there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2143. The suggestion or motivation to combine references must be found in the prior art. MPEP 2143 citing *In re Vaeck*, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

The Office Action states that it would have been obvious to modify Matsumura "by including therein data timing means as taught by Manning" whereby "Compressed test data can thus be read at successive clock edges despite the command requiring a plurality of clock edges." Manning, column 5, lines 35-38; Office Action, page 2. This is not a motivation to modify Matsumura.

Matsumura shows a clock synchronous memory and in Figures 21-22 a compression circuit 4j. The compression circuit 4j is described in Matsumura from column 21, line 16 to column 22, line 25. The compression circuit 4j of Matsumura compresses 256 bits down into a

single bit ECMP with EXOR circuits 4j0-4j7 and an AND circuit 4ja. The single bit ECMP is then transferred through a latch 4k to a pad 8p.

Matsumura shows compressing 256 bits into a single bit ECMP, and there is no reason to read the single bit ECMP at successive clock edges as described in Manning. No more information from the single bit ECMP could be read by modifying Matsumura according to Manning. One skilled in the art would not have been motivated to modify Matsumura to read the single bit ECMP at the successive clock edges of Manning.

Furthermore, Matsumura describes a DDRSDRAM and data transfer in synchronization with the rising and falling of a clock signal. Matsumura, column 22, lines 27-45. Matsumura does not mention transmitting the single bit ECMP in relation to the rising and falling of a clock signal. One skilled in the art would not have been motivated to do something that Matsumura did not do even when data transfer in synchronization with the rising and falling of a clock signal was known to Matsumura. The Office Action has not identified evidence of a motivation to modify Matsumura.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 1-2, 4-6, 8-10, 12-28, 31-41, and 43-45 has not been established in the Office Action, and that claims 1-2, 4-6, 8-10, 12-28, 31-41, and 43-45 are in condition for allowance.

Claim 30 recites a memory device comprising a plurality of memory cells, means for compressing a plurality of data values read from selected ones of the memory cells into test data, and means for producing the test data on edges of a clock signal.

Claim 30 is a means-plus-function claim under 35 U.S.C. § 112, paragraph 6. MPEP 2181. The Office Action has not presented an explanation or a rationale as to why the showing of Matsumura or Manning is equivalent to the corresponding elements disclosed in the specification as is required by MPEP 2182 and 2183.

Claims 3, 7, 11 and 29 were rejected under 35 USC § 103(a) as being unpatentable over Matsumura, Manning, and Schober (U.S. Patent No. 6,297,668). The applicant respectfully traverses.

Schober issued on 2 October 2001, which is after the 29 January 1999 filing date of the above-identified application. The applicant does not admit that Schober is prior art.

The Office Action states that it would have been obvious to modify the procedure in Matsumura and Manning to provide "race-free" flip-flops and avoid error in flip-flop operation. Office Action, pages 3-4. The Office Action did not identify flip-flops in Matsumura or Manning that suffered from the error in flip-flop operation identified by Schober. The text from Schober does not provide a motivation for modifying either Manning or Matsumura.

The applicant respectfully submits that a *prima facie* case of obviousness of claims 3, 7, 11 and 29 has not been established in the Office Action, and that claims 3, 7, 11 and 29 are in condition for allowance.

RESPONSE UNDER 37 CFR § 1.111
Serial Number: 09/239898
Filing Date: January 29, 1999
Title: METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE WITH COMPRESSED DATA USING A SINGLE OUTPUT

Page 18
Dkt: 303.550US1

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

MIRMAJID SEYYEDY ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
612-373-6973
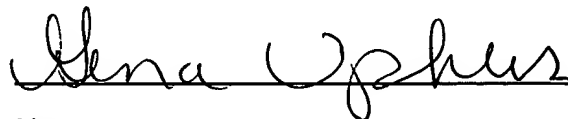
Date 1 JULY 2003   By _____
                              Robert E. Mates
                              Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this ___ day of July, 2003.

Gina M. Uphus

Name

Signature